

An Oracle White Paper
February 2011

Scaling Throughput and Managing TCO with Oracle's Netra SPARC T3-1 Servers

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Executive Overview

Skyrocketing growth in user volumes and the trends toward integration of wireless, video, multimedia, and messaging technologies are forcing telecommunications companies to rapidly expand their IT infrastructures to meet new application demands. To help telecommunications providers address the challenge of scaling throughput while also managing TCO, Oracle has introduced the Netra SPARC T3-1 server, a carrier-grade 2RU rack-mountable Netra server that features the powerful and energy-efficient SPARC T3-1 processor. The SPARC T3 processor is based on the Ultra SPARC T2 processor, and doubles the available CPU cores and threads, making it easy for telecommunications providers to cost-effectively scale their IT infrastructure within existing datacenter space, power, and cooling limitations.

Introduction

In a period of intense competition and emerging technologies, telecommunications companies face the challenge of delivering and supporting a multitude of new voice and data solutions. Although many IT managers must quickly and dramatically scale datacenter resources to address growing applications needs, they must do so within tight constraints of operating budgets and available floor space.

For this reason, Oracle's strategy focuses on engineering innovative processors and systems with robust compute, memory, and I/O densities to provide higher levels of throughput—higher by orders of magnitude than existing systems. At the same time, Oracle's ecocentric design choices drastically change typical assumptions for required power and cooling. In pursuit of these goals, Oracle has introduced a third-generation processor that leverages chip multithreading (CMT)—the SPARC T3 processor with CoolThreads technology. Designed to deliver high throughput within a small power envelope the SPARC T3 processor incorporates up to 16 cores and 128 processor threads, delivering breakthrough application throughput—up to twice the throughput of the previous UltraSPARC T2 processor. In addition, the SPARC T3 processor uses the increased transistor budget resulting from the use of a 40 nm silicon

technology to implement the industry's first massively threaded system-on-a-chip (SoC). Among other new features, the SPARC T3 processor includes on-chip Level 1 and Level 2 caches as well as a newly designed floating point pipeline that is available in each processor core.

Oracle's new Netra SPARC T3-1 servers combine the ruggedness, NEBS level 3 certification, and reliability of earlier Netra server designs with the performance and ecoefficiency of SPARC T3 processors. The Netra SPARC T3-1 servers use a compact 2U-form-factor chassis that features remarkable expansion capabilities for memory, I/O, and storage. The resulting ruggedized server offers a dramatic boost in throughput capacity while lowering operating costs and conserving energy and space—at the same time enhancing availability even within challenging environmental conditions.

Oracle's Netra SPARC T3-1 Server

The Netra SPARC T3-1 server offers extreme reliability and high throughput, while at the same time offering unprecedented processor core, memory, and I/O densities for dramatic expansion and configuration flexibility. This rack-mountable NEBS server comes in a compact 2RU form factor and leverages a commercial SPARC T3-1 motherboard with a single socket SPARC T3 processor.

The CoolThreads chip multithreading (CMT) technology in the SPARC T3 processor helps to deliver high throughput for demanding telecommunications applications while minimizing power consumption. (The section “The Evolution of Throughput Computing” describes the evolution of CMT and explains how CMT improves application throughput while maintaining a low power envelope.) The SPARC T3 processor in the Netra SPARC T3-1 server is based on Oracle's second-generation CMT processor design. It leverages the same CoolThreads technology proven in the Netra T5220 server based on the previous-generation UltraSPARC T2 processor. The SPARC T3 processor in the Netra SPARC T3-1 server—with up to 16 cores and 128 concurrent processor threads—takes throughput-per-watt to a new level, doubling the throughput of the earlier UltraSPARC T2 processor. It adds on-chip networking and improved floating-point capabilities to address the demands of intensive packet processing and multimedia processing workloads.

In addition to breakthrough performance and scalability, the Netra SPARC T3-1 server is certified to meet Network Equipment Building Specification (NEBS) Level 3 requirements for environments that demand continuous availability and simplified management. NEBS Level 3 certification (not merely compliance) indicates that the system has undergone a series of rigorous, independently conducted tests to prove that it can continue to operate under severe environmental conditions.

Numerous architectural features—including key redundant and hot-swappable components—enable the Netra SPARC T3-1 server to deliver outstanding levels of availability and reliability that contribute to continuous system operation. Redundant hot-swappable DC or AC power supplies and hot-pluggable disk drives, for example, help to enhance system uptime. A built-in service processor with Integrated Lights Out Manager (ILOM) capabilities enables remote monitoring and system management, providing the kind of reliability and serviceability needed by telecommunications companies or military organizations that operate in severe environments.

The Netra SPARC T3-1 server delivers scalability, energy efficiency, and reliability for a variety of demanding applications:

- Media gateway controllers
- Operations and maintenance for telecommunications networks
- Signaling gateways
- Intelligent networks
- Multimedia Messaging Service (MMS)/Short Message Service (SMS) and unified messaging

- Defense/military/intelligence applications including shipboard command and control, mobile weapons control, and remote intelligence access servers
- Embedded original equipment manufacturer (OEM) applications, such as industrial process control, semiconductor test equipment, and network imaging systems
- Application servers
- Web servers
- Content caching, network proxy servers
- Home/visitor location registries (HLR/VLR)
- Base station controllers (BSCs)
- Content distribution networks
- DNS services
- Firewalls for virtual private network/IP security (VPN/IPSEC)
- IP traffic management systems
- Security systems
- Streaming media systems
- OSS/BSS

Key Features

Key features of the Netra SPARC T3-1 server include the following:

- Up to 128 simultaneous execution threads using CoolThreads CMT technology with 16 SPARC cores in the SPARC T3 processor at 1.65Ghz. The processor contains an L2 cache, memory access crossbar, 1 floating point unit per core, and 2 FBDIMM2 memory controllers
- Telecordia NEBS Level 3 certification for extremely reliable operation in harsh environmental conditions
- Enhanced system uptime with Dry Contact Alarms (DCAs); on-chip reliability, availability, and serviceability (RAS) features; redundant AC or DC power supplies; hot-pluggable disk drives; support for hardware RAID (0 + 1); and redundant hot-swappable fan modules
- Exceptional expandability and I/O performance, featuring five PCI-Express (PCIe) 3 PCIe (Supports two Full height half length PCIE cards on mezzanine tray) and two XAUI slots, four onboard 10/100/1,000-Mb/sec Ethernet ports, and 16 DDR3 Memory modules/memory slots (for a maximum of 256 GB using 16 GB DDR3-DIMMs)
- Large internal storage capacity, with a maximum of four internal, 2.5-inch, 300 GB, hot-pluggable (SAS) disk drives with DVD-RW.
- A compact rack-optimized 2U design

- Simplified state-of-the-art remote maintenance with Integrated Lights Out Manager (ILOM)
- Preloaded with the Oracle Solaris operating system to shorten time to deployment

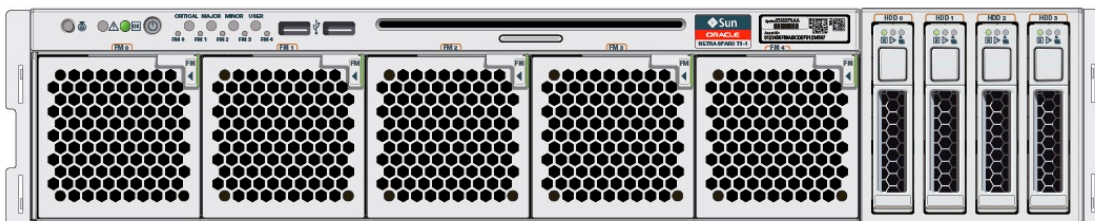


Figure 1. The Netra SPARC T3-1 server enclosure has a compact rack-optimized design.

Designed to complement the rest of Oracle's carrier-grade server family, the Netra SPARC T3-1 server addresses the dynamic and emerging needs of telecommunications providers:

- **Efficient application scalability.** With support for 128 threads and large memory capacity, Netra SPARC T3-1 servers integrate 10 Gb Ethernet (10 GbE), I/O, and cryptographic acceleration directly onto the SPARC T3 processor chip. This approach contributes to leading levels of performance and scalability for packet processing and media processing workloads, while maintaining extremely high efficiency.
- **Leading ecoresponsibility.** Netra SPARC T3-1 servers continue a tradition of ecoresponsibility by offering optimal performance and performance-per-watt across a wide range of workloads. The SPARC T3 processor incorporates unique power management features at both processor core and memory levels. High-efficiency power supplies and an innovative chassis design (with hexagonal suction holes that optimize airflow) help to minimize the need for cooling and lower energy costs.
- **System reliability.** Reliability features help to increase availability, reduce costs, and meet SLA targets, even in harsh operating environments. NEBS Level 3 certification demonstrates that the system has been rigorously tested and can withstand severe operating conditions. With high levels of integration provided by the SPARC T3 processor design, the Netra SPARC T3-1 server has a relatively small part count and is designed specifically for high RAS levels. Redundant, hot-swappable AC or DC power supplies, fan modules, and disk drives enhance reliability and serviceability. Low power consumption reduces generated heat loads and the possibility of temperature-related problems.
- **Simplified management.** Each Netra SPARC T3-1 server provides an ILOM service processor. ILOM provides a command-line interface (CLI), a Web-based graphical user interface (GUI), and Intelligent Platform Management Interface (IPMI) functionality to support out-of-band monitoring and administration.
- **Industry-leading tools for virtualization and consolidation.** The Netra SPARC T3-1 server is ideal for consolidation, providing low-level multithreading support for virtualization at multiple layers of the technology stack. Oracle VM Server for SPARC (previously called Sun Logical Domains) exploits the thread-intensive model of the SPARC T3 processor because they allow

multiple instances of Oracle Solaris to run concurrently, while Oracle Solaris Containers provide virtualization within a single Oracle Solaris instance.

- **Zero-cost security.** With electronic intrusion and theft at all-time highs, secure communications and data protection have never been more important. Because each SPARC T3 processor features up to sixteen integrated cryptographic accelerators, there is no need to transmit plain text on the network or to store plain text in storage systems. Netra SPARC T3-1 servers can support more cryptographic operations per second than many competitive systems and dedicated cryptographic accelerator cards, with minimal impact to system overhead.
- **Accelerated time to deployment.** Netra SPARC T3-1 servers running Oracle Solaris 10 provides full binary compatibility with earlier UltraSPARC systems, preserving investments and speeding time to deployment. Oracle's CoolTools for SPARC help to accelerate application selection, profiling, testing, tuning, debugging, and deployment. Netra SPARC T3-1 servers come preinstalled with Oracle Solaris 10 to expedite deployment and provide a robust and secure operating environment.

The Evolution of Throughput Computing

Traditional high-frequency, single-threaded processor designs offer little hope for improvement over time in real-world application performance. For many processor designs, ramping up clock rates yields only small gains in performance while consuming significantly more power and generating large heat loads that require extensive cooling. Rising power and cooling requirements translate into escalating energy costs that take an increasingly large bite out of IT operating budgets, which are often already flat or shrinking.

For this reason, Oracle's Netra servers have been engineered with processors and systems that provide higher throughput—higher by orders of magnitude than for existing systems—at the same time drastically reducing requirements for power and cooling. This focus on throughput computing is a composite strategy targeted at improving the performance of key workloads:

- CMT processor designs (such as the SPARC T3 processor) provide massive thread-level parallelism (TLP) and increase application throughput, at the same time maintaining attractive power and cooling profiles.
- Innovative and secure, Oracle Solaris 10 effectively delivers the resources of CMT processors to applications, facilitating fine-grained system virtualization and high utilization while maintaining binary compatibility for Oracle Solaris applications running on SPARC processor-based platforms.
- Oracle's compilers, development tools, APIs, and system engineering efforts leverage CMT processor capabilities, resulting in significant application performance gains.

This section describes the limitations of traditional processor designs and how Oracle's emphasis on CMT can increase real-world application performance while optimizing energy and space efficiency.

Moore's Law and Diminishing Returns of Traditional Processor Design

An often-quoted tenet of Moore's Law states that the number of transistors that fit in a square inch of integrated circuitry will double approximately every two years. For more than three decades, the pace of Moore's Law has held, driving processor performance to new heights. Processor manufacturers have long exploited these gains in chip real estate to build increasingly complex processors, with instruction-level parallelism (ILP) as a goal. Today, these traditional processors employ very high frequencies along with a variety of sophisticated tactics to accelerate a single instruction pipeline, including

- Large caches
- Superscalar designs
- Out-of-order execution
- Very high clock rates
- Deep pipelines
- Speculative prefetches

Although these techniques have produced faster processors with impressive-sounding multigigahertz frequencies, they have largely resulted in complex, hot, and power-hungry processors that don't fit well within the constraints of today's datacenters. In fact, many workloads are simply unable to take advantage of the hard-won ILP provided by these processors. Applications with high shared memory and data requirements are typically more focused on processing a large number of simultaneous threads (or TLP) rather than running a single thread as quickly as possible, as in ILP-centric workloads.

Making matters worse, the majority of ILP in existing applications has already been extracted, and further gains are likely to be small. With higher clock speeds, each successive processor generation has seemingly demanded more power than the last, and microprocessor frequency scaling has leveled off in the range of 2 to 4 GHz as a result. Deploying pipelined superscalar processors requires more power, which limits the approach because of a fundamental need for processor cooling.

Chip Multiprocessing with Multicore Processors

To address this limitation, some microprocessor engineers have used the transistor budget provided by Moore's Law to group two or even four conventional processor cores on a single physical die, creating multicore processors (or CMP). The individual processor cores introduced by many CMP designs have no greater performance than previous single-processor chips and in fact have been observed to run single-threaded applications more slowly than single-core processor versions. However, aggregate chip performance increases because multiple programs (or multiple threads) can be accommodated in parallel (or TLP).

Unfortunately, most currently available (or soon-to-be-available) chip multiprocessors simply replicate cores from existing single-threaded processor designs. This approach typically yields only slight improvements in aggregate performance, because it ignores key performance issues such as memory speed and hardware thread context switching. As a result, although these designs provide some

additional throughput and scalability, they can still consume considerable power and generate significant heat.

Chip Multithreading with CoolThreads Technology

There is a disparity between processor speeds and memory access rates. Although processor speeds continue to double every two years, memory speeds have typically doubled only every six years. As a result, memory latency now dominates much application performance, erasing even very impressive gains in clock rates. This growing disconnect is the result of memory suppliers focusing on density and cost rather than speed.

Unfortunately, this relative gap between processor and memory speeds can leave ultrafast processors idle as much as 85 percent of the time, waiting for memory accesses to return required data. Ironically, as traditional processor execution pipelines get faster and more complex, the effect of memory latency grows—fast, expensive processors spend more cycles waiting and doing nothing. Worse still, idle processors continue to draw power and generate heat. It is easy to see that frequency (for example, gigahertz) is truly a misleading indicator of real performance.

First introduced with the UltraSPARC T1 processor, CMT takes advantage of CMP evolution but adds a critical capability—the ability to scale with threads rather than frequency. Unlike traditional single-threaded processors and even most current multicore (or CMP) processors, hardware multithreaded processor cores allow rapid switching between active threads as other threads stall for memory. Figure 2 illustrates the difference between CMP, fine-grained hardware multithreading (FG-MT), and CMT. The key to the CMT approach is that each core is designed to switch between multiple threads on each clock cycle. As a result, the processor's execution pipeline remains active doing useful work, even as memory operations for stalled threads continue in parallel.

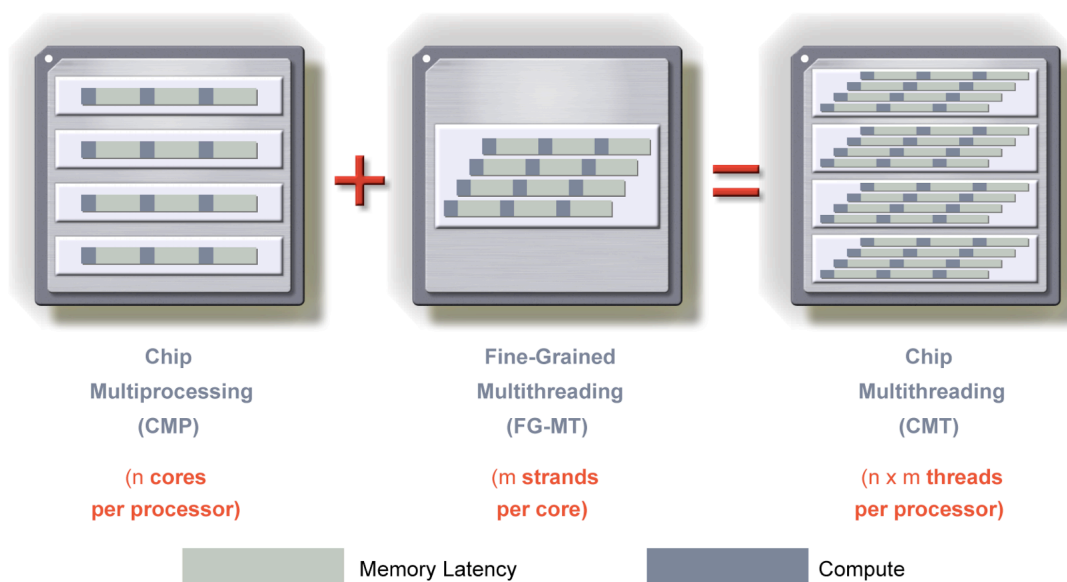


Figure 2. Chip multithreading combines chip multiprocessing and fine-grained hardware multithreading.

CMT provides value by increasing the execution pipeline's ability to do useful work on any given clock cycle. Pipeline utilization is greatly enhanced because a number of execution threads now share resources. The negative effects of memory latency are effectively masked because the processor and memory subsystems remain active in parallel to the execution pipeline. Because individual processor cores implement much simpler pipelines (emphasizing TLP over ILP), they are also substantially cooler and require significantly less electrical energy to operate. This innovative approach results in CoolThreads technology—multiple physical instruction execution pipelines (one for each core), with multiple active thread contexts available per core.

SPARC T3 Processors with CoolThreads Technology

The SPARC T3 processor is based on UltraSPARC T2 processor, and doubles the available CPU cores and threads. The processor contains 16 SPARC cores each of which can run 8 threads concurrently. The processor contains an L2 cache, memory access crossbar, 2 FBDIMM2 memory controllers, and 1 FPU per core. The processor is optimized for highly threaded transactional processing whereby the core utilization is maximized due to the minimization of the time waiting on memory accesses.



Figure 3. The UltraSPARC T2 (left) and SPARC T3 processors take advantage of CoolThreads technology.

TABLE 1. A SIDE BY SIDE COMPARISON OF ULTRASPARC T2 AND SPARC T3 FEATURES

FEATURE	ULTRASPARC T2 PROCESSOR	SPARC T3 PROCESSOR
Year introduced	2007	2010
Cores per processor	Up to 8	Up to 16
Threads per core	8	16
Threads per processor	64	128
Hypervisor	Yes	Yes
Chip memory characteristics	4 memory controllers, 16 DIMMs per controller	2 memory controllers, 16 DIMMs per controller
Caches	16-KB instruction cache, 8-KB data cache, 4-MB L2 cache (8 banks, 16-way associative)	16-KB instruction cache, 8-KB data cache, 6-MB L2 cache (16 banks, 24-way associative)
Technology	65-nm technology	40-nm technology

TABLE 1. A SIDE BY SIDE COMPARISON OF ULTRASPARC T2 AND SPARC T3 FEATURES

FEATURE	ULTRASPARC T2 PROCESSOR	SPARC T3 PROCESSOR
Floating-point unit (FPU)	1 FPU per core, 8 FPUs per chip	1 FPU per core, 16 FPUs per chip
Integer resources	2 integer execution units per core	2 integer execution units per core
Cryptography	Stream-processing unit per core, support for the 10 most popular ciphers	Enhanced Stream-processing unit per core for the most popular ciphers
Additional on-chip resources	Dual 10 GbE interfaces, integrated PCIe controller	Dual 10 GbE interfaces, integrated PCIe controller

Taking Chip-Multithreaded Design to the Next Level

The design team for the SPARC T3 processor started with these key goals in mind:

- Increasing computational capabilities to meet growing throughput demands by providing twice the throughput of the UltraSPARC T2 processor
- Supporting larger and more-diverse workloads with greater floating-point performance
- Powering faster networking to serve new network-intensive content
- Providing end-to-end datacenter encryption
- Increasing service levels and reducing downtime
- Improving datacenter capacities while reducing costs

CMT architecture is ultimately very flexible, allowing different modular combinations of processors, cores, and integrated components. The considerations listed above drove an internal engineering effort that compared different approaches with regard to making improvements on the successful UltraSPARC T2 architecture. For example, simply increasing the number of cores would have gained additional throughput but would have resulted in consuming extra die area, leaving no room for integrated components such as floating-point processors.

System on a Chip (SoC) Design

Unlike complex single-threaded processors, CMT processors utilize the available transistor budget to implement multiple hardware multithreaded processor cores on a chip die. In particular, the SPARC T3 processor uses the available transistor budget to implement the industry's first SoC, including:

- Up to sixteen cores at 1.65 GHz
- Sixteen threads per core for a maximum of 128 threads per processor
- On-chip Level-1 and Level-2 caches
- Two memory controllers for on-chip support of as many as 256 DDR3-DIMMs
- Sixteen fully pipelined FPUs (1 per core)
- Per-core cryptographic acceleration

- Two on-chip 10 GbE interfaces
- Integrated PCIe interface

The SPARC T3 processor design recognizes that memory latency is truly the bottleneck to improving performance, allowing each core to switch between up to eight threads. By increasing the number of threads supported by each core, the SPARC T3 is able to provide approximately twice the throughput of the UltraSPARC T2 processor. Each SPARC T3 processor provides up to sixteen cores, with each core able to switch between up to sixteen threads (128 threads per processor). In addition, each core provides two integer execution units, so that a single UltraSPARC core is capable of executing two threads at a time.

SPARC T3 Processor Architecture

The SPARC T3 processor extends Oracle's throughput computing initiative with an elegant and robust architecture that delivers real performance to applications. A high-level block diagram of the SPARC T3 processor is shown in Figure 4.

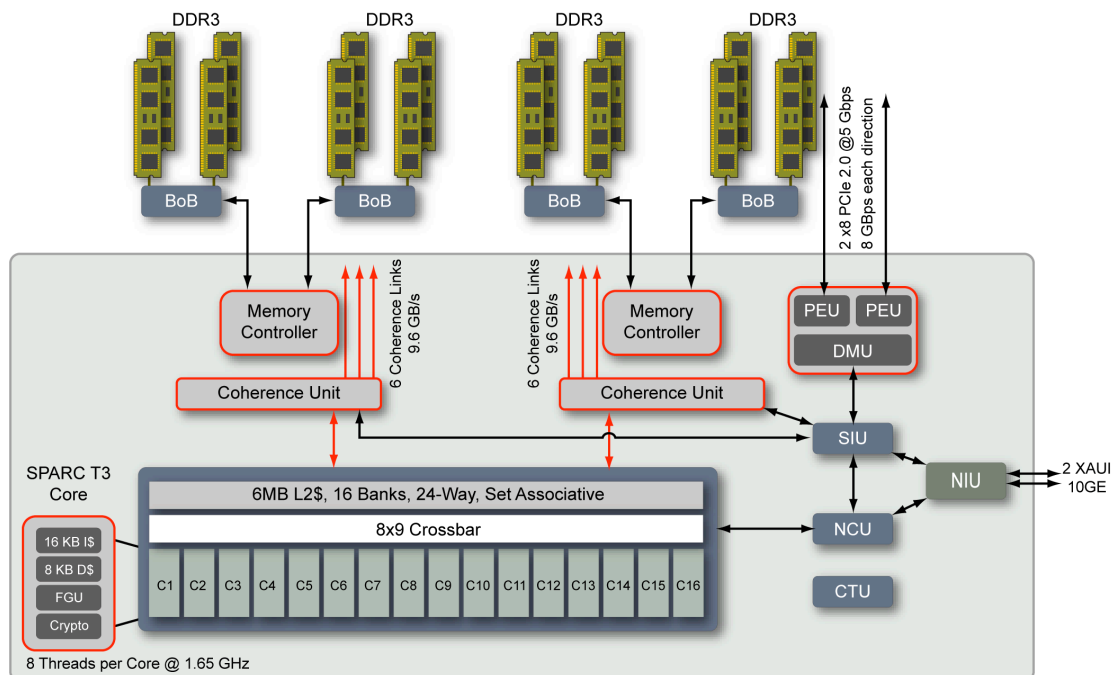


Figure 4. The SPARC T3 processor combines sixteen cores, memory management, cryptographic support, 10 GbE, and PCIe on a single chip.

The SPARC T3 processor is the industry's first 16 core processor with 128 threads incorporated into a design that integrates all the key functions of a system into a single processor: computing, networking, security, and I/O, all powered by Oracle Solaris. Used in Oracle's SPARC T3 servers, it delivers the scalability and performance you need to meet next generation computing requirements for Web services, middleware applications, and OLTP databases.

Each core provides its own fully pipelined floating-point and graphics unit, as well as a stream-processing unit (SPU). The FPUs greatly enhance floating-point performance over that of the UltraSPARC T2, enhancing the performance of multimedia processing including image encoder/decoder (codec) operations. The SPUs provide wire-speed cryptographic acceleration with over 10 popular ciphers supported, including DES, 3DES, AES, RC4, SHA-1, SHA-256, MD5, RSA to 2048 key, ECC, and CRC32. (In contrast, the UltraSPARC T1 processor supports only two ciphers—DES and 3DES.) Embedding hardware enhanced cryptographic acceleration for many ciphers in the SPARC T3 processor allows end-to-end encryption with no penalty in either performance or cost.

Key Features of the Netra SPARC T3-1 Server

Netra SPARC T3-1 servers are designed to leverage the considerable resources and power of the SPARC T3 processor. These carrier-grade servers mark a departure from traditional system designs and take advantage of specific SPARC T3 processor features, including 128 threads, large on-chip memory capacities, cryptographic acceleration, integrated on-chip 10-GbE networking and I/O technology, and power management. In a compact, energy-efficient, 2U package, Netra SPARC T3-1 servers provide high performance within significant power, cooling, and space constraints—at the same time enabling remarkable reliability, density, and expandability.

Keeping Up with Application Growth Through System Expansion

The Netra SPARC T3-1 server offers dramatic flexibility for expansion to help telecommunications companies keep up with application growth without requiring a major system upgrade. With support for 16 DDR3 DIMM memory slots, the server supports memory expansion up to 256 GB (using 16 GB DIMM modules). Up to 1.2 TB of internal disk can also be configured into the system using four 2.5" SAS-2 300 GB drives. This dramatic expansion and configuration flexibility is combined with an Integrated Lights Out Manager (ILOM 3.0) service processor and the proven reliability of Netra carrier-grade systems to help telecommunications companies reduce TCO for their IT infrastructure.

Reduced Management Costs with Integrated Lights Out Manager (ILOM)

An important component of TCO is the cost of managing IT servers. The Netra SPARC T3-1 server provides an Integrated Lights Out Manager (ILOM 3.0) service processor to simplify remote management. The Integrated Lights Out Manager provides a command-line interface (CLI), a Web-based graphical user interface (GUI), and Intelligent Platform Management Interface (IPMI) functionality to aid out-of-band monitoring and administration.

Configuration Details

The table below details the physical and architectural aspects of the system.

TABLE 2. FEATURES OF NETRA SPARC T3-1 SERVERS

FEATURE	NETRA SPARC T3-1 SERVER
CPU	SPARC T3 processor at 1.65 GHz with 16 cores
Threads	Up to 128 threads with 16 cores
Memory capacity	16 slots with up to 256 GB maximum (using 16-GB DDR3-DIMMs)
Internal storage	Up to 4 2.5-inch SAS 300-GB disk drives (hardware RAID 0/1) with DVD-RW
Removable media	DVD-RW
USB	4 USB 2.0 ports (bootable)
PCI expansion	5 PCIe slots: 2 full-height, half-length, 64-bit at 133MHz 3 low-profile or 1 Low profile and 2-XAUI combo slots (x8 connector)
Ethernet	4 onboard GbE ports (10/100/1,000)
Power supplies	2 hot-swappable AC or DC 1200-W power supply units (N+1 redundancy)
Fans	5 hot-swappable fan modules
Form factor	2U
Operating system	Oracle Solaris 10 (preinstalled)
System management	ILOM, accessible via network or serial management ports
Telco features	Dry Contact Alarms (DCAs), DB-15 connector NEBS Level 3 certified

Conclusion

Oracle's Netra SPARC T3-1 servers offer incredible reliability and system density—with robust compute, memory, networking, storage, and I/O capabilities in a small, compact 2U form factor. Leveraging SPARC T3 processor technology and engineering expertise in chassis and systems design, these platforms deliver new levels of performance—and new levels of performance-per-watt—in a rackmountable, NEBS-certified system. Deploying these servers can create a more agile and reliable infrastructure that scales easily to deliver new, integrated multimedia application services within a small footprint, while at the same time delivering needed mission-critical service levels.

Netra SPARC T3-1 servers provide expandable, high-capacity resources for demanding Web infrastructure, database, and server consolidation and virtualization initiatives. This server will suit network infrastructure applications like OSS/BSS, BRM, and media gateway controller. These carrier-grade systems are ideal for installations where reliability, performance, density, and energy conservation are paramount. Given the high throughput capabilities and energy efficiency of these servers, IT departments can easily consolidate workloads and improve utilization, while at the same time preserving investments in applications.



Scaling Throughput and Managing TCO with
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January 2011

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Hardware and Software, Engineered to Work Together