Scaling Down From Chip Multi-core to Single Core – The OpenSPARC T1 Experience

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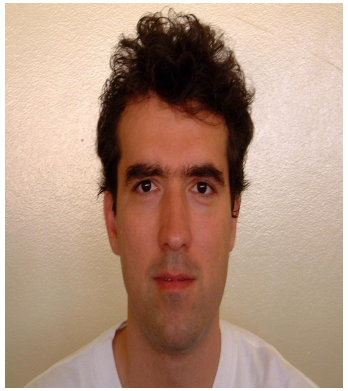
Development Team



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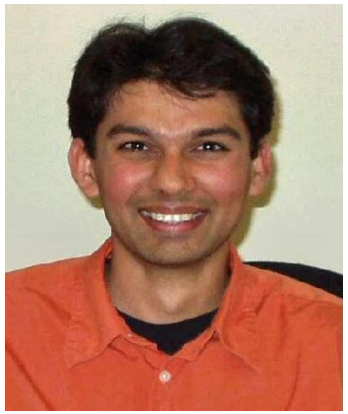

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World's First Open Source Microprocessor

solaris™ OpenSPARC™

OpenSPARC.net

- Governed by GPL (2)
- Complete chip architecture
- Register Transfer Logic (RTL)
- Hypervisor API
- Verification suite and architectural models
- Simulation model for Solaris bringup on s/w
- 4700+ downloads worldwide

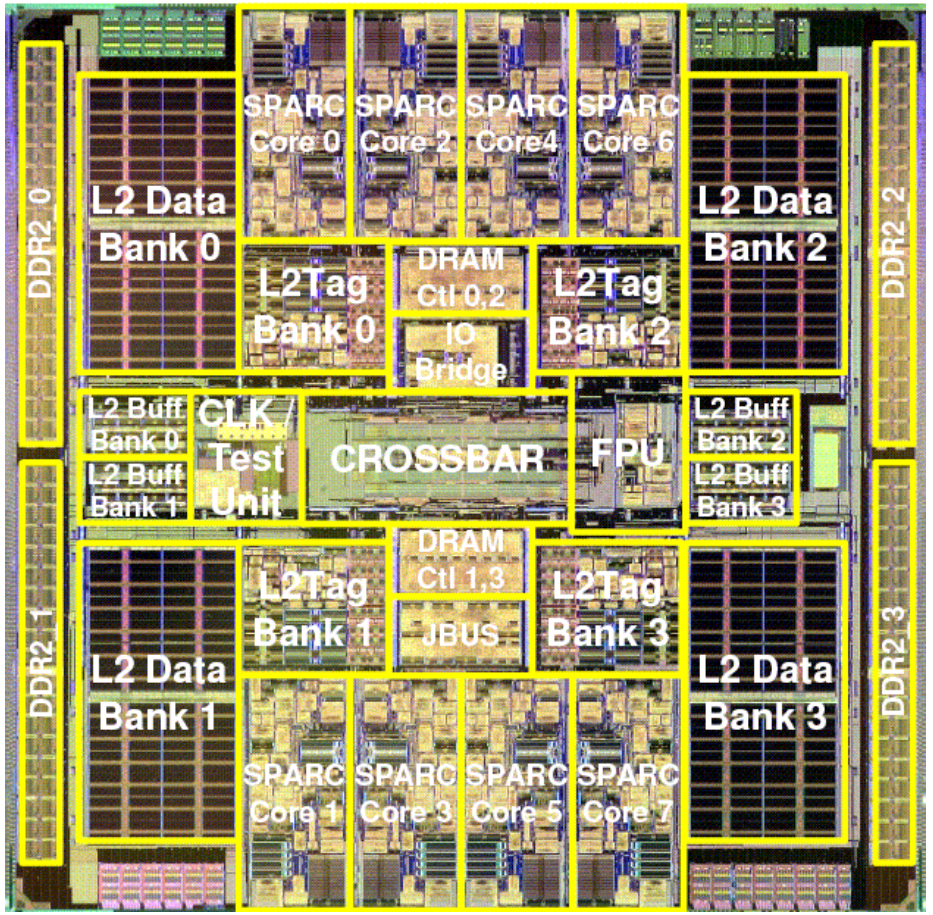
Linux

BSD

Agenda

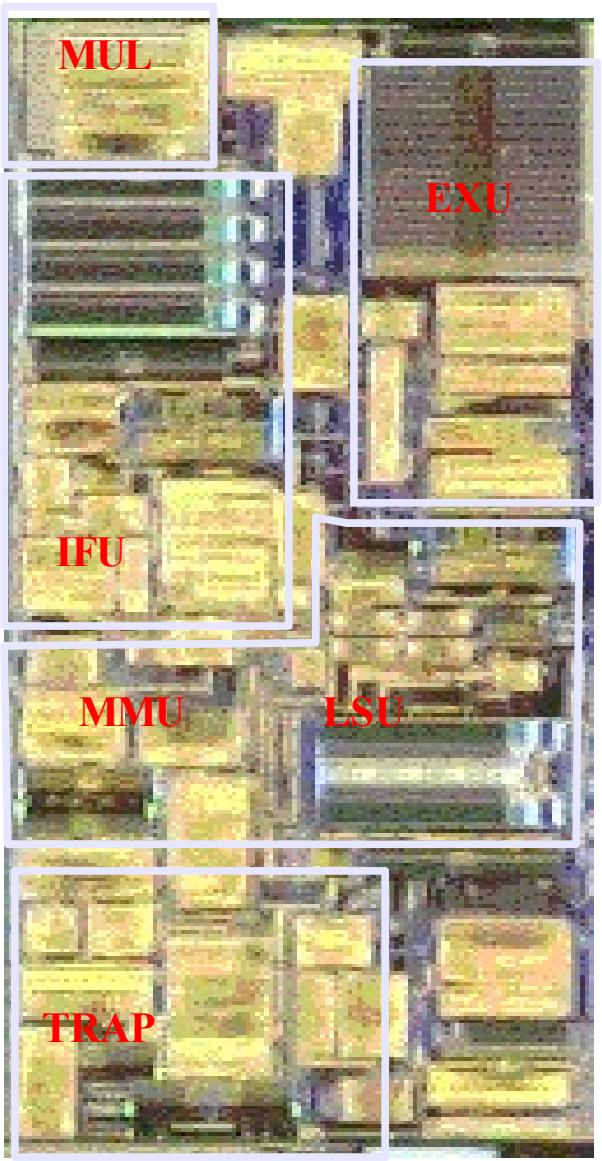
- OpenSPARC T1 Primer
- Single Core Single Thread implementation
  - Motivation
  - New Features
  - Results
  - Availability
- Future Development/Research Opportunities
- Q & A

OpenSPARC T1



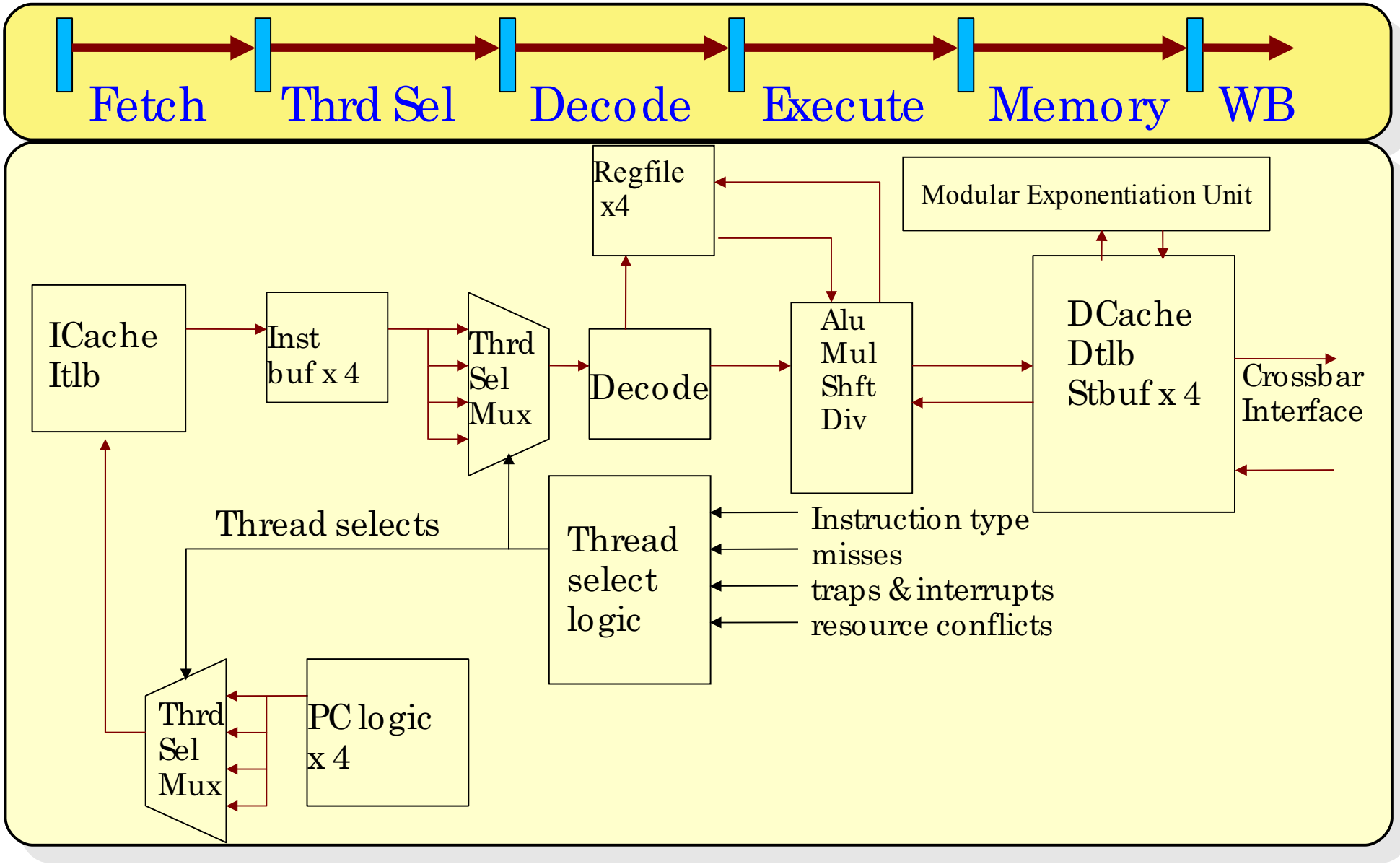
- SPARC V9 implementation
- Eight cores, four thread each – 32 simultaneous threads
- Simpler core architecture to maximize cores on die
- Caches, dram channels shared across cores give better area utilization
- Shared 12 way set associative 3MB on-chip L2
- 378mm2 die in 90nm dissipating ~70W
- ~300M transistors

UltraSPARC-T1 Processor Core



- Four threads per core
- Single issue 6 stage pipeline
- 16KB I-Cache, 8KB D-Cache
- Unique resources per thread
  - Registers
  - Portions of I-fetch datapath
  - Store and Miss buffers
- Resources shared by 4 threads
  - Caches, TLBs, Execution Units
  - Pipeline registers and DP
- Core Area = 11mm2 in 90nm
- MT adds ~20% area to core

SPARC Core Pipeline



Motivation

- Create configurability for wider research
  - Originally custom design
  - Allow community to select parameters on the fly
- Create simple core
  - Based on feedback from Universities
- Feedback from RAMP
  - Create small core for thousand way systems
  - http://ramp.eecs.berkeley.edu/

Objective

- Create implementation of OpenSPARC T1 that provides
  - Small area foot-print
  - Friendly to FPGA map
  - Complete verification environment
  - Expandability for multi-core, multi-thread designs
  - Out-of-the box experience
- (Longer Term) Demonstrate system that
  - Includes peripherals (e.g. DRAM)
  - Is capable of booting commercial OS
  - Costs few hundred dollars (At least to Universities)

Implementation

- Three orthogonal optimizations
  - Single thread core of OpenSPARC T1
  - FPGA implementations of custom design blocks (e.g. SRAMs)
  - Ability to remove Modular Arithmetic Unit
- Three optimizations combined provide smallest possible area foot-print

Single thread T1

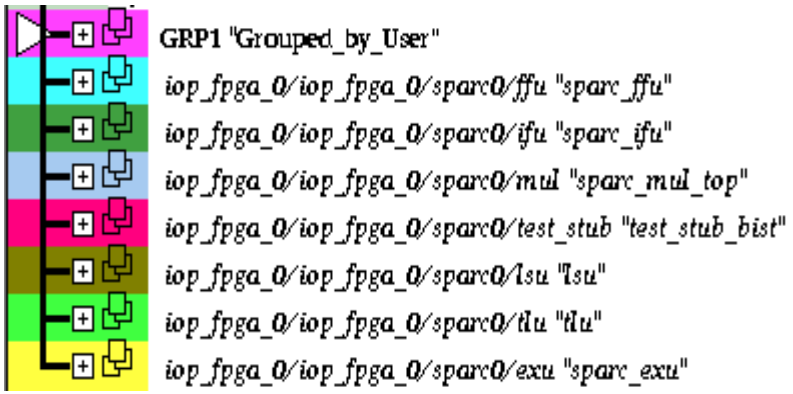
- Conditionally removed multi-thread logic in majority of the blocks
- Significant saving in area due to removal of large per thread data-paths and thread-select multiplexers
- Redesign of Integer Register File to remove number of write access ports
- Configurable design
  - Can choose 4-thread or 1-thread at the synthesis time
- Area saving of about 40%

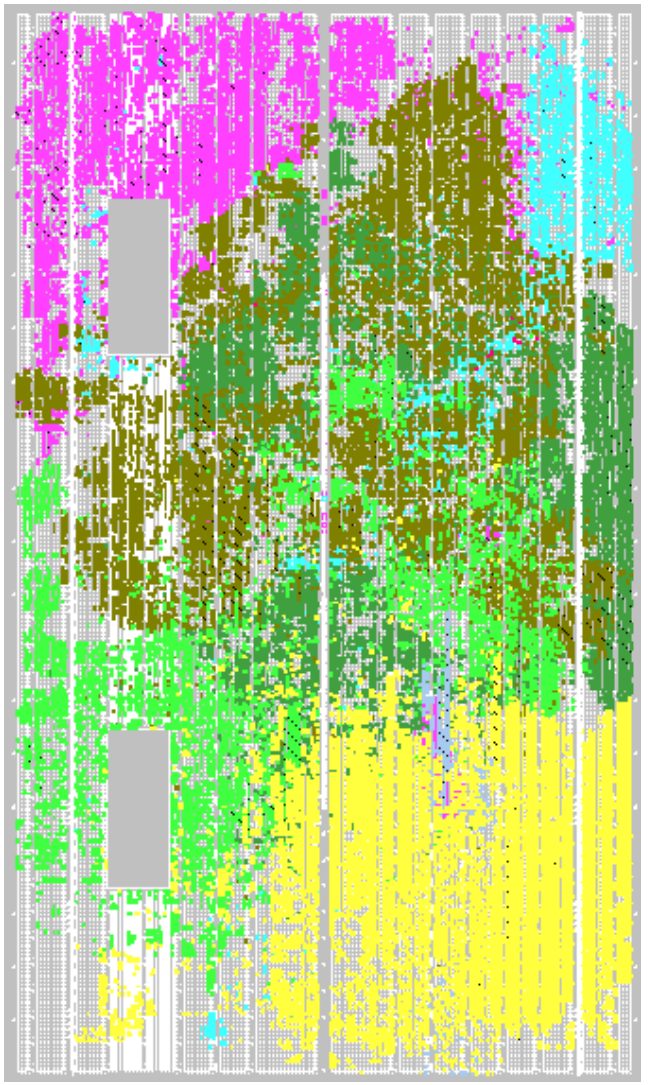
FPGA synthesis

- Re-coding of custom blocks and SRAM arrays to use FPGA resources (Block RAMs, Flop elements)
  - Icache, Dcache tag and data arrays
  - Store buffer, Integer register file, Floating point register file
  - L2Cache data and tag array
- Re-coding of multiplier to utilize FPGA resources
- Removal of asynchronous elements of the design
  - Latches, gated clocks
- Reduced TLB size from 64-entry to 8-entry
- About 40% saving in the area

Results (1)

- Synthesis on Xilinx XC4VFX100-11FF1152
  - 39,084 LUTs (44%)
  - 123 BRAMs – 16KB (30%)
  - 50MHz operation
  - Synthesis time – 25 minutes
  - Place and Route time – 42 minutes





Results (2)

Design	LUTs	Block RAMs	Latches	Comments
4-thread SPARC core (Before)	135190	4	3123	OpenSPARC T1 v 1.3
4-thread SPARC core (After)	70152	127	0	OpenSPARC T1 v1.4 FPGA_SYN opt
1-thread SPARC core (After)	39084	123	0	OpenSPARC T1 v1.4 FPGA_SYN, 1THREAD, and NO_CRYPTO

Results from Synplicity Sinplify Pro v5.8 on Virtex-4 devices

- Functionally clean
  - Passes verification suit that is part of OpenSPARC T1

What is Available

- OpenSPARC T1 hardware bundle, includes
  - Configurable design for single-thread SPARC core
  - Configurable design for FPGA implementation
  - Verification suit
    - Three to choose from: fullchip, core1 (4-thread), and 1-thread
    - Netlist verification environment
  - Documents
- OpenSPARC T1 software bundle, includes
  - Architectural simulator, Full system simulator

Future Directions (1)

- Efficient Multi-Threaded (MT) processor on FPGAs
  - Very interesting for hardware emulation
- Most blocks scale between 30-35% for 4-thread MT
  - Except Execute Unit – analyze bottlenecks

Blocks	Single thread	Four thread	MT Overhead
Fetch	7432	10210	0.27
Execute	12252	31018	0.61
Load/Store	9559	12939	0.26
Trap Logic	5727	8410	0.32
Floating point frontend	2168	2388	0.09

Future Directions (2)

- Create Multi-core solutions
  - Include coherency
- Add new instructions
  - e.g. Transactional Memory instructions
- Heterogeneous CMT
- Add application specific coprocessors
- Build system and boot OS
  - Stay tuned

Conclusion

64-bit SPARC processor for FPGAs

Comes in two flavors -

1-thread and 4-thread

Available now, for free at

www.opensparc.net

(Architects Wanted)

Thank You!

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