Multi-Core Expo
March 29, 2007

OpenSPARC
Open Source Hardware - Myth Becomes Reality

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OpenSPARC & SPARC CMT Technology
Sun Microsystems

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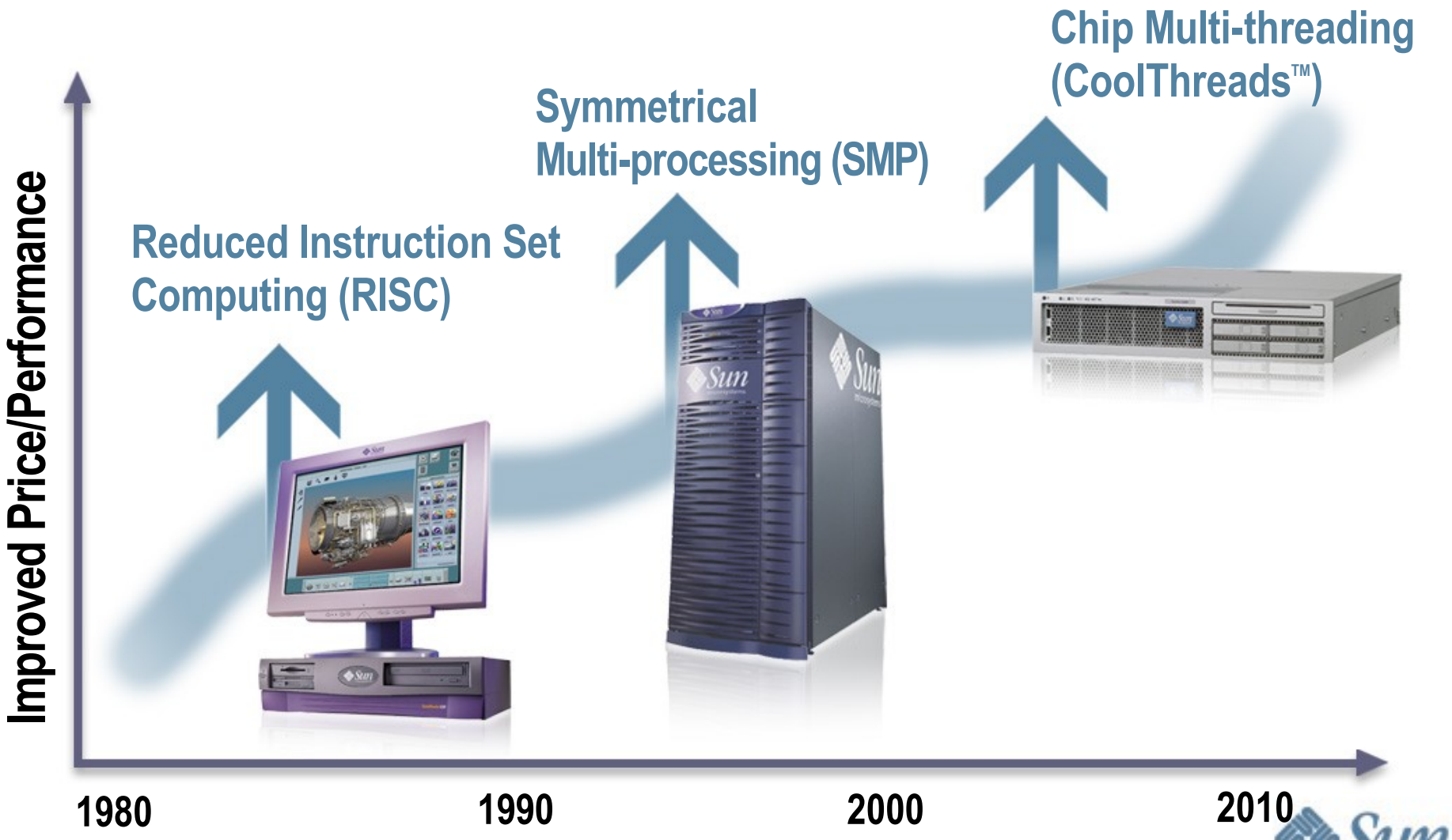
The Waves of Computing



Big Bang is here – Web 2.0

Network Computing Is Thread Rich

Web services, Java™ applications, database transactions, ERP . . .

Moore's Law

A fraction of the die can already build a good processor core; how am I going to use a billion transistors?

Worsening Memory Latency

It's approaching 1000s of CPU cycles! Friend or foe?

Growing Complexity of Processor Design

Forcing a rethinking of processor architecture – modularity, less is more, time-to-market

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Enabling The Participative Infrastructure

- Microprocessor Innovation with massive multithreading
- Power of communities. Innovation matters more than ever !....and more innovation to be had by the power of communities
  - > Software (Java, OpenSolaris and Linux) and now Hardware - OpenSPARC
- Prevalent high bandwidth fueling efficient collaborative design work

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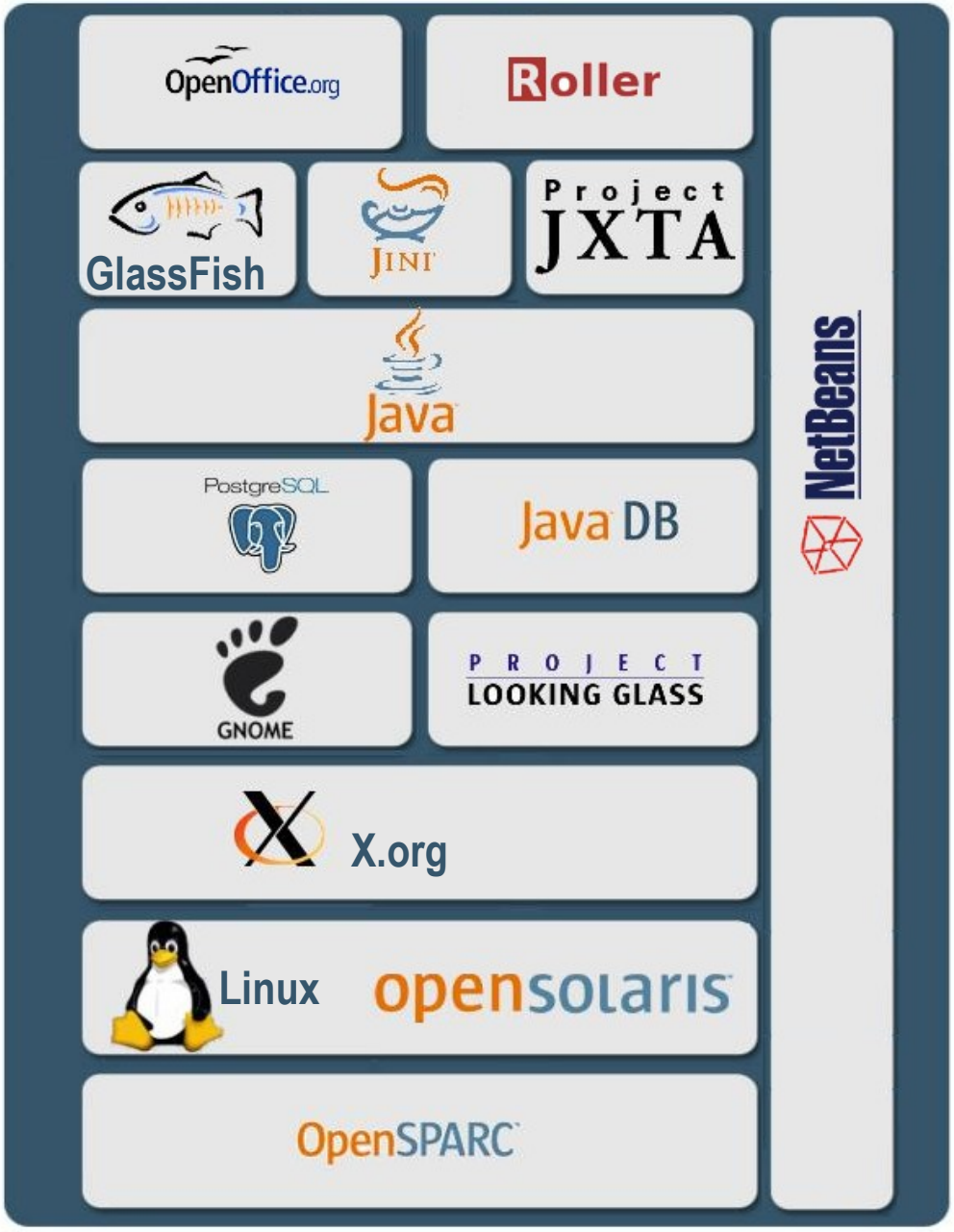
Implications on SoC designs

- Need for a new ecosystem to take advantage of new highly threaded architectures
  - CAD Tools
  - Integration and test suites.
  - Compilers, debuggers, etc.
- Integrateable architecture, i.e. Standard based interfaces for building blocks integration
- Ability to innovate freely within and outside the CPU core – key to enabling and growing new market applications
- Ability to cooperate freely as a community – eliminating IP sharing barriers is key to accelerate innovation

Openness in Hardware Industry

- **Open Formats – provides access to data (read/write)**
  - e.g GDSII, SPICE format, LEF, DEF,
- **Open Standards – provides choice to users**
  - e.g Verilog, VHDL, System Verilog, Property Specification Language (PSL)
- **Open Source – opportunities for developers**
  - Distribute binaries and source code
  - Freely modifiable and re-distribute
  - Meritocracy, Peer Review/Public discussion
  - Ok to make money, but not for access to code
  - e.g OpenSPARC, Open Verification Library (OVL)

Sun's Open Source Stack



OpenSPARC Community

Sharing Creates Communities
Communities Create Markets

World's First Open Source Multicore/Multithreaded Microprocessor

OpenSPARC.net

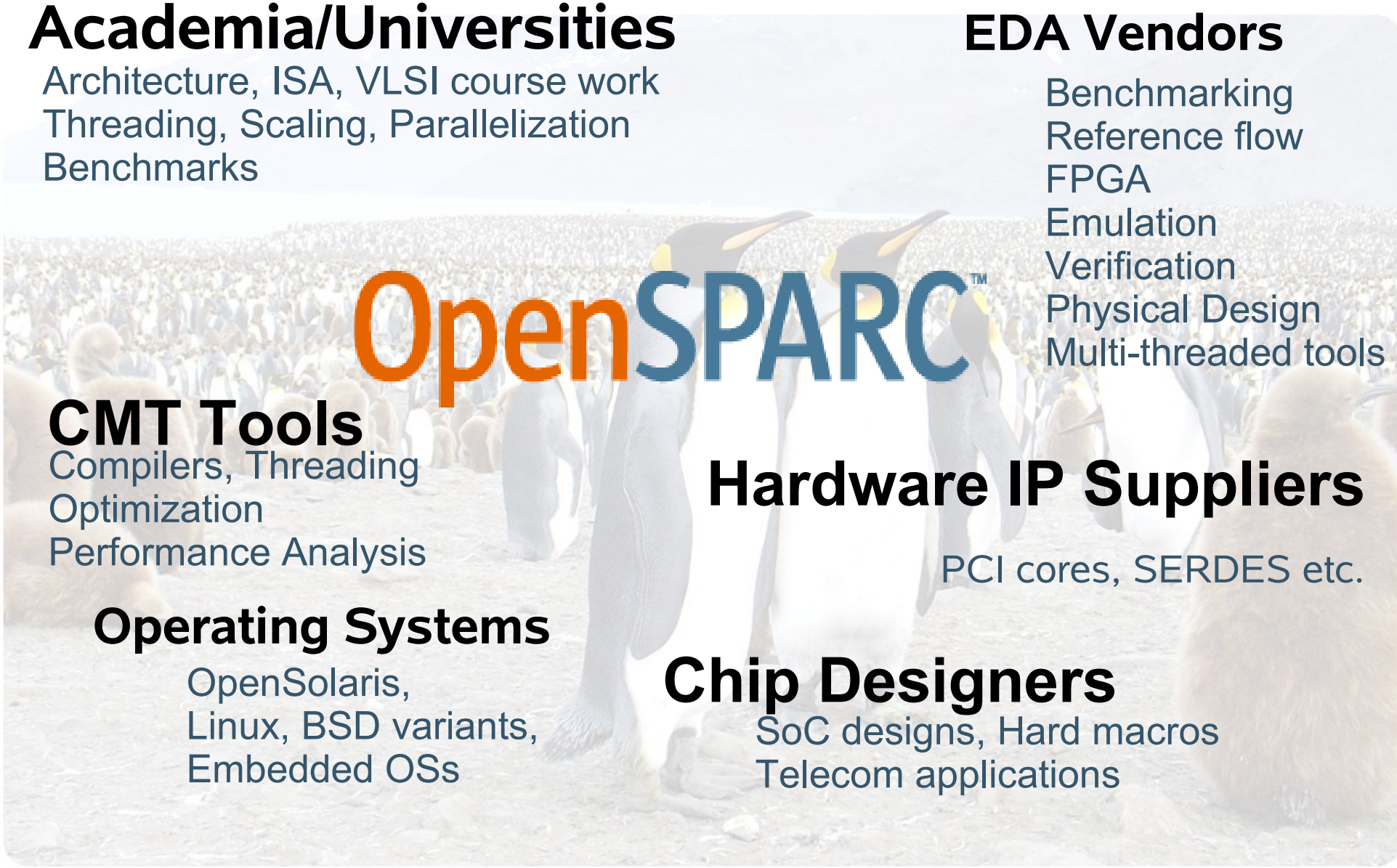
- Governed by GPL (2)
- Complete chip architecture
- Register Transfer Logic (RTL)
- Hypervisor API
- Verification suite and architectural models
- Simulation model for Solaris bringup on s/w

solaris™ OpenSPARC™

Linux

BSD

OpenSPARC Communities



Academia/Universities

Architecture, ISA, VLSI course work
Threading, Scaling, Parallelization
Benchmarks

EDA Vendors

Benchmarking
Reference flow
FPGA
Emulation
Verification
Physical Design
Multi-threaded tools

OpenSPARC™

CMT Tools

Compilers, Threading
Optimization
Performance Analysis

Hardware IP Suppliers

PCI cores, SERDES etc.

Operating Systems

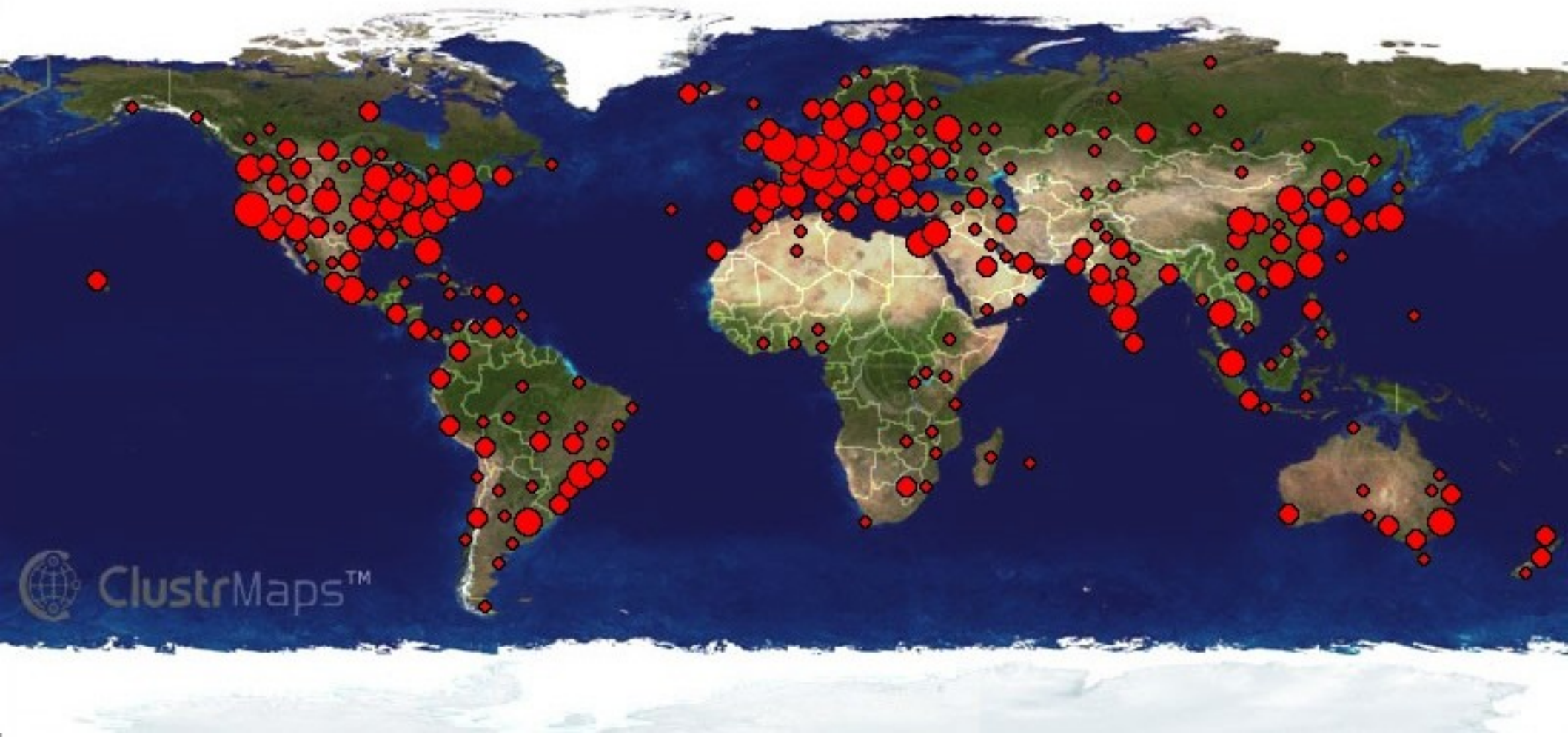
OpenSolaris,
Linux, BSD variants,
Embedded OSs

Chip Designers

SoC designs, Hard macros
Telecom applications

About the Community: opensparc.net

Clustermaps for http://opensparc.net



Innovation Happens Everywhere

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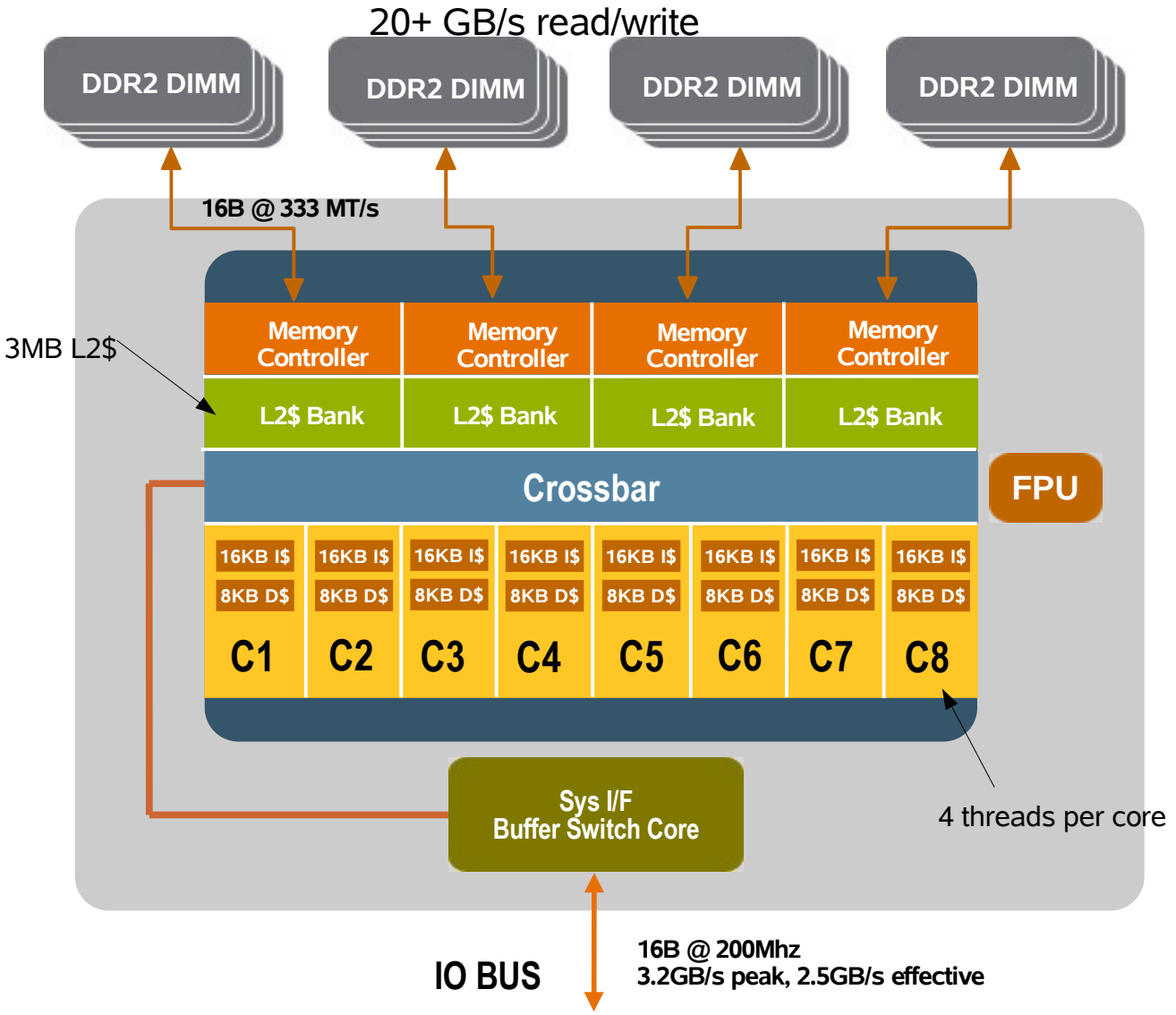
OpenSPARC™

Building the Community

Over 4500 OpenSPARC Downloads To Date
Roughly 400 unique visitors per Week
Global Reach (North America, Europe, Asia)
Established Governance Board
including LSI Logic and Nathan Brookwood, Insight64

Get the Source, Start Innovating



Things you can do:

- use as is
- add/delete cores
- add new instr.
- change FPU
- add video/graphics
- add network interface
- change memory interface
- change I/O interface
- change cache/mem interface
- etc.

Innovate anywhere – within or outside

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OpenSPARC T1 for Hardware Engineering

- Chip Design/Verification Package Includes
  - (14 million lines of code!)
  - Chip RTL design
  - Verification environment
  - Verification test suites
  - Synthesis scripts for all RTL
  - SPARC Architecture simulator
  - Documentation
  - Synplicity scripts for FPGA implementation of SPARC core, Crossbar, FPU

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OpenSPARC T1 for Software Engineering

- Architecture and Performance Modeling Package includes:
  - SAM – SPARC instruction-accurate full-system simulator (includes source code)
  - SAS - Instruction-accurate SPARC Architecture Simulator (includes source code)
  - Solaris Images for simulation:
    Solaris 10, Hypervisor, OBP images
  - Legion – SPARC full-system simulation model for Software Developers (includes source code)
  - Hypervisor source code
  - Documentation

OpenSPARC.net: Help drive innovation

- Contribute to platform projects
  - FreeBSD
  - Linux
- Contribute code to Cool Tools
- Design new uses to the 32 threads
- Envision the next camera, cell phone, or PDA
  - i.e. SimplyRISC and others…

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OpenSPARC

First 64-bit, 32 Thread Architecture RTL code available under GPLv2 license

Community-driven ports of GNU/Linux to OpenSPARC, including Ubuntu

Inclusion of OpenSPARC as the "textbook" chip design at many universities

Broad support from Design Houses, Fab Companies and Tools companies

Community-driven ports of GNU/Linux to OpenSPARC, including Ubuntu

3rd Parties are discounting software to OpenSPARC members

"Sun's decision to release Verilog source code for the UltraSPARC hardware design under a free software license is an historic step - Sun is showing its profound understanding of the forces shaping our technological future in making this decision."

Eben Moglen
Software Freedom Law Centre

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